

WHAT IS CLAIMED IS:

1. A semiconductor device having a memory array, comprising:
a plurality of substantially parallel word lines;
a plurality of substantially parallel bit lines, wherein each of the plurality of the word lines is substantially perpendicular to each of the plurality of the bit lines;
a first dummy word line disposed at a periphery of the memory array, wherein the first dummy word line is substantially parallel to the plurality of word lines and overlaps at least two non-adjacent bit lines.
2. The device as claimed in claim 1, wherein the first dummy word line comprises polysilicon.
3. The device as claimed in claim 1, further comprising a second dummy word line substantially parallel to the first dummy word line, wherein the second dummy word line is disposed at a periphery of the memory array opposite from the first dummy word line.
4. The device as claimed in claim 3, wherein the second dummy word line overlaps at least one bit line.
5. The device as claimed in claim 4, wherein the second dummy word line overlaps at least two non-adjacent bit lines
6. A semiconductor device, comprising:
a memory array comprising a plurality of transistors; and
a plurality of non-memory transistors,
wherein the memory array includes
a plurality of substantially parallel word lines,

a plurality of substantially parallel bit lines, each of the plurality of the word lines being substantially perpendicular to each of the plurality of the bit lines, and

a first dummy word line disposed at a periphery of the memory array, wherein the first dummy word line is substantially parallel to the plurality of word lines and overlaps at least one of the plurality of bit lines.

7. The device as claimed in claim 5, wherein the first dummy word line comprises polysilicon.

8. The device as claimed in claim 5, further comprising a second dummy word line formed substantially parallel to the first dummy word line, wherein the second dummy word line is disposed at a periphery of the memory array opposite from the first dummy word line.

9. The device as claimed in claim 7, wherein the second dummy word line overlaps at least one of the plurality of bit lines.

10. The device as claimed in claim 8, wherein the first dummy word line overlaps at least two non-adjacent bit lines.

11. The device as claimed in claim 9, wherein the second dummy word line overlaps at least two non-adjacent bit lines.

12. A method for manufacturing a semiconductor device, comprising:
forming a plurality of substantially parallel bit lines;

forming a plurality of substantially parallel word lines, wherein each of the plurality of the word lines is substantially perpendicular to each of the plurality of the bit lines;

depositing a layer of tetraethyl orthosilicate over the plurality of bit lines and plurality of word lines, wherein the amount of tetraethyl orthosilicate deposited on top of the plurality of word line having a thickness greater than half the distance separating adjacent word lines; and
etching back the tetraethyl orthosilicate layer.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com